module sim\_Control();

reg [3:0]opcod;

wire RegDest;

wire ALUSrc;

wire MemToReg;

wire RegWrite;

wire MemWrite;

wire Branch;

wire ALUop2;

wire ALUop1;

wire ALUop0;

wire Jump;

Control uut(opcod[3:0], RegDest, ALUSrc, MemToReg, RegWrite, MemWrite, Branch, ALUop2, ALUop1, ALUop0, Jump);

initial

begin

#1 opcod = 0;

#1 opcod = 1;

#1 opcod = 2;

#1 opcod = 6;

#1 opcod = 7;

#1 opcod = 8;

#1 opcod = 10;

#1 opcod = 14;

#1 opcod = 15;

#1 opcod = 0;

end

endmodule